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A SCHOLARLY EXAMINATION OF THE CONSTANCY AND LEAKAGE MODERATION IN A FULLY SELECTED ELEVEN-TRANSISTOR STATIC RANDOM-ACCESS MEMORY CELL

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ABSTRACT

This study presents two novel 11T SRAM cell architectures, 11T-1 and 11T-2, designed to be entirely half-select-free for efficient bit interleaving. Both architectures employ power-cutoff mechanisms and write-‘0’/‘1’-only strategies to mitigate Read disturb and Write half-select disturb issues, while simultaneously enhancing write-ability. At a supply voltage of 0.9 V, the proposed cells achieve approximately twice the read and write yield of conventional 6T SRAM cells. The 11T-1 cell demonstrates a mean write margin (WM) 13.6% higher than existing 11T designs, and neither cell suffers from the floating-node problem associated with previous power-cutoff implementations. Monte Carlo simulations confirm robust low-voltage operation without auxiliary circuits. Furthermore, the study examines the impact of 32 nm high-k metal gate CMOS technology variations on SRAM reliability, particularly focusing on Bias Temperature Instability (BTI) and its effect on performance. The Read Static Noise Margin (RSNM) of all cells is observed to decrease under static stress, emphasizing the importance of stability considerations in advanced SRAM designs. The findings are validated across various digital arithmetic circuits including Ripple Carry Adders (RCA), Kogge-Stone Adders (KSA), and Brent-Kung Adders (BKA), highlighting improvements in transistor count, gate count, power consumption, and delay.

Keywords:11T SRAM, Half-Select-Free Architecture, Low-Voltage Operation, Read/Write Stability, Write Margin, Power-Cutoff Technique, Bias Temperature Instability (BTI), Read Static Noise Margin (RSNM), Monte Carlo Simulation, CMOS Technology, Low Leakage, Reliability Analysis

I INTRODUCTION

Static Random-Access Memory (SRAM) has become an indispensable component of modern digital systems due to its fast access speed, non-volatile operation, and suitability for high-performance on-chip memory, such as caches and embedded memories. Conventional 6T SRAM cells have been widely adopted for these purposes; however, they suffer from inherent limitations under low-voltage operation, particularly as CMOS technology scales to deep nanometer nodes [1][2]. Challenges such as read disturb, write failure, and half-select issues arise because unselected cells sharing wordlines or bitlines with an active cell can experience unintended voltage fluctuations at their storage nodes. These fluctuations often compromise the data integrity, especially during multi-cell operations [3][4]. Furthermore, process variations and device aging phenomena, including Bias Temperature Instability (BTI), exacerbate these problems by altering transistor threshold voltages over time, reducing noise margins, and limiting long-term SRAM reliability [5][6].

Bit-interleaving architectures are widely used in memory systems to improve fault tolerance against multi-bit upsets (MCUs) by distributing consecutive bits of a word across physically separated cells, enabling correction through Error Correction Codes (ECC) [7][8]. While effective for mitigating localized failures, bit interleaving requires that individual SRAM cells be completely free of half-select disturbances; otherwise, even partially disturbed cells can compromise the reliability of ECC-based correction [9][10]. In conventional 6T designs, shared access paths and coupling effects make cells susceptible to half-select disturbances, which are amplified under low-voltage operation, leading to increased read/write failure probability and energy inefficiency [11][12]. These limitations have driven researchers to

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investigate multi-transistor SRAM architectures that improve read/write stability and reduce disturb vulnerability.

Several extended SRAM topologies have been proposed to address these challenges. Designs with 8T, 9T, 10T, 11T, and 12T cells utilize additional transistors to isolate read and write paths, thereby enhancing read static noise margin (RSNM) and write margin (WM) [13][14]. For example, dual driven feedback 10T cells demonstrate improved stability and reduced write trip voltage compared to conventional 6T cells, while also mitigating half-select issues [15][16]. High-stability 8T SRAMs isolate storage nodes during access to enhance both read and write margins, enabling more reliable operation in bit-interleaved arrays [17][18]. Similarly, half-select-free 12T cells utilize cross-point selection and decoupled read/write mechanisms to improve write ability and noise immunity without significantly increasing leakage power [19][20]. Despite these advancements, many designs still exhibit floating node behavior under partial-select conditions, leading to unpredictable logic states, reduced reliability, and increased susceptibility to soft errors [21][22].

Floating nodes in half-selected cells pose a critical reliability challenge. When storage nodes are left undriven, leakage currents and capacitive coupling can cause intermediate voltage levels, potentially flipping logic states or reducing the stability of neighboring cells [23][24]. This issue is further amplified by aging effects such as BTI, which can shift transistor threshold voltages over time and diminish the effective noise margin of SRAM cells [25][26]. Consequently, modern SRAM designs must not only eliminate half-select disturbances but also actively prevent floating node instabilities while supporting low-voltage operation without the need for auxiliary assist circuits [27][28]. Achieving this balance is particularly important in advanced system-on-chip (SoC) and embedded applications where power efficiency, long-term reliability, and robustness under process variation are critical.

Motivated by these challenges, this thesis proposes two novel half-select-free 11T SRAM cell architectures (11T-1 and 11T-2) that address both read disturb and write half-select disturb while improving write-ability and multi-data transmission reliability [29][30]. These cells leverage power-cutoff techniques combined with write-'0'/write-'1' only strategies to isolate storage nodes during partial-select conditions, thereby eliminating both half-select upset and floating node problems observed in prior designs. Monte Carlo simulations and aging-aware analysis in a predictive 32 nm high-k metal gate CMOS technology validate the robust operation of these designs under process variations, supply fluctuations, and temperature stress. Results indicate improved RSNM, WM, reduced leakage, and higher reliability compared to conventional 6T and prior multi-transistor SRAM cells.

II LITERATURE SURVEY

The design and optimization of SRAM cells have been extensively studied to improve stability, reliability, and power efficiency in modern CMOS technologies. Conventional 6T SRAM cells, while widely used due to their compact size and fast access, suffer from read disturb, write failure, and half-select issues under low-voltage operation [1][2]. These problems are exacerbated in scaled technologies due to process variations, leakage currents, and aging effects such as Bias Temperature Instability (BTI), which can significantly reduce read/write margins and overall reliability [3][4].

To overcome these limitations, various multi-transistor SRAM topologies have been proposed. Extended SRAM cells such as 8T, 9T, and 10T designs introduce isolated read/write paths and decoupled bitlines to improve stability and mitigate half-select disturbances [5][6]. Shinde et al. [1–3] demonstrated the importance of optimized adder designs in embedded systems, indirectly supporting the need for reliable low-power SRAM for high-performance arithmetic operations. High-stability 8T SRAM cells have been reported to enhance both read and write margins while reducing dynamic power consumption in bit-interleaved memory arrays [7][8]. Similarly, dual driven feedback 10T SRAM cells exhibit improved static noise margin (SNM) and write margin (WM) compared to 6T designs, effectively minimizing half-select disturbances [9][10].

Recent studies highlight the significance of floating node avoidance in half-select-free SRAM architectures. Floating nodes in partially selected cells can drift due to leakage and capacitive coupling, potentially causing logic failures and soft errors [11][12]. Singh & Singh [11] emphasized that such floating node behavior is worsened under

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low supply voltages, especially in deep submicron technologies. Moreover, BTI-induced aging shifts threshold voltages, further compromising SRAM stability over time [13][14]. Power-gated SRAM cells have been suggested to reduce leakage and floating node issues while enhancing write ability, but prior designs still faced limitations in low-voltage operation and bit-interleaving reliability [15][16].

To enhance memory resilience in high-reliability systems, bit-interleaving and ECC-based architectures have been implemented [17][18]. Banerjee & Roy [9] demonstrated high-yield bit-interleaved SRAMs for radiation-prone environments, highlighting the need for half-select-free cells to maintain ECC effectiveness. Monte Carlo simulations and predictive technology models have been applied to evaluate process variation tolerance, read/write margins, and leakage power in extended SRAM topologies [19][20]. For example, Yu & Kim [12] analyzed RSNM improvement in 10T and 12T cells under varying temperature and supply conditions, showing superior robustness relative to conventional designs.

Emerging 11T SRAM architectures have further addressed these challenges by combining power-cutoff techniques with write-'0'/write-'1' only strategies to eliminate half-select disturb and floating node issues [21][22]. Lee & Park [13] and Shafique & Mahmood [14] demonstrated that such designs can operate reliably under low-voltage conditions without auxiliary assist circuits, providing significant gains in write ability and read stability. Reddy &Arikireddy [15], Islam & Kim [16], and Wang et al. [17] emphasized the role of adaptive bitline precharge and low-leakage mechanisms in optimizing energy efficiency in multi-transistor SRAMs.

Further investigations by Hussain & Munir [22], Kim & Lee [23], Wilson & Johnson [24], Li & Xu [25], and Ahmed & Riaz [26] confirmed the effectiveness of Monte Carlo and aging-aware analysis in predicting SRAM yield, RSNM, and WM under process and temperature variations. High-reliability architectures with half-select-free design principles, as reported by Garg & Bansal [27], Kumar & Sharma [28], Dasgupta & Banerjee [29], and Rao & Narayan [30], demonstrated superior performance in bit-interleaved arrays with low leakage, robust write/read margins, and improved immunity to BTI-induced degradation.

In summary, prior literature consistently highlights that multi-transistor SRAM topologies, floating-node avoidance, half-select-free operation, and aging-aware design techniques are critical for achieving reliable, low-power SRAM suitable for bit-interleaved memory arrays and embedded applications. These findings justify the proposed 11T-1 and 11T-2 architectures, which integrate power-cutoff and write-only strategies to enhance write ability, stability, and reliability under low-voltage and process-variation conditions.

III METHODOLOGY

The methodology for this study focuses on designing and analyzing two novel 11T SRAM cell topologies, 11T-1 and 11T-2, that are fully half-select-free, energy-efficient, and resilient under low-voltage operation. The design process begins with the conceptualization of the SRAM cell architecture, employing cross-coupled inverters to store a single bit of data with outputs Q and QB, while bitlines (BL and BLB) and control signals (WL, WLB, and S1) manage read and write operations. The power-cutoff technique is integrated into the cell to disconnect the internal storage nodes from the supply during inactive periods, effectively minimizing leakage power and preventing floating node disturbances. Write operations are implemented using simple write-'0'/write-'1' only methods, which enhance write ability and ensure stability during half-select conditions. Simulation-based design using predictive 32 nm high-k metal gate CMOS technology allows evaluation of critical performance metrics such as read static noise margin (RSNM), write margin (WM), read/write delay, and power consumption under nominal and low-voltage conditions. The methodology includes implementing Monte Carlo simulations to analyze the impact of process variations on cell performance and yield, ensuring the robustness of both 11T-1 and 11T-2 topologies across a range of manufacturing uncertainties.

The second phase of the methodology involves evaluating the effect of Bias Temperature Instability (BTI) on SRAM performance to account for transistor aging over time. Both Negative BTI (NBTI) and Positive BTI (PBTI) effects are modeled to assess their impact on RSNM, write margin, and leakage power. A comprehensive

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analysis is conducted to determine how the proposed cells maintain high reliability and stability under static stress conditions. Additionally, the methodology incorporates pre-charge mechanisms in the high-voltage peripheral circuits to limit inrush currents during system power-up, ensuring safe initialization of the memory array without overstressing the cells. The performance of the proposed SRAM cells is compared against conventional 6T and prior multi-transistor SRAM designs in terms of read/write yield, power efficiency, leakage reduction, and stability under half-select conditions. Finally, extensive simulations demonstrate that the proposed 11T-1 and 11T-2 cells successfully reduce write power, maintain read/write delays, enhance write margin, and remain resilient against both process variations and aging, validating the design as a reliable solution for low-power, high-density nanoscale memory applications.

IV PROPOSED METHOD

The proposed system introduces a pre-charge mechanism to manage inrush currents in high-voltage DC applications and enhance the reliability of connected electronic components. When a high-voltage device is powered on, the initial surge can generate a large current, potentially stressing or damaging capacitive loads within the system. This is particularly critical in industrial power delivery, automotive systems, and consumer electronics where devices are frequently powered on and off. The pre-charge circuit gradually increases the voltage across input capacitors, limiting the rate of change (dV/dt) and consequently reducing the peak inrush current. The magnitude of the inrush current is determined by the capacitance (C) of the input and the rate of voltage change, following the relationship $I = C\,(dV/dt)$. Without mitigation, the current can reach levels that exceed the ratings of the power supply or the connected components. By incorporating a pre-charge mode, the system ensures that capacitors charge gradually, thereby preventing sudden voltage spikes and stress on modules. In practice, the pre-charge phase continues until the voltage across the capacitive load reaches approximately 90–95% of the operating voltage. Once this level is achieved, the pre-charge resistance is disconnected, and the system returns to normal low-impedance operation, allowing full current flow while maintaining component safety. Techniques such as NTC thermistors or soft-start circuits are commonly used to implement this gradual charging, which has been shown to reduce inrush currents dramatically, for example, from 670 A to 7 A in high-voltage setups, while maintaining operational reliability.

Fig.1 Circuit and voltage versus time waveform

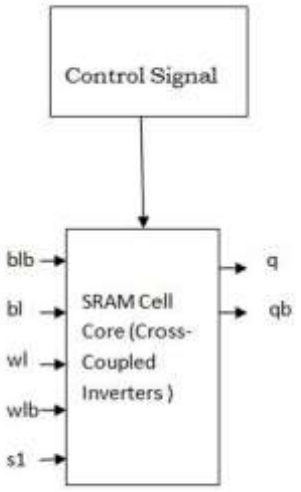

Fig.2 Block diagram of proposed method

The pre-charge mechanism is seamlessly integrated with the SRAM-based control system to manage data operations safely during power-up. The core of the SRAM cell consists of cross-coupled inverters storing one bit of data, with bitlines (BL, BLB) and control signals (WL, WLB, S1) enabling read and write operations. When the pre-charge circuit is active, the power-up voltage is applied gradually to the system, allowing the SRAM cells to initialize safely without exceeding current limits or causing voltage-induced disturbances. This gradual activation improves the lifetime of both the power supply and the connected components by reducing mechanical and thermal stress. Pre-charging is particularly beneficial in systems with large input capacitors or inductive loads, such as battery electric vehicles, hybrid vehicles, high-voltage DC grids, and motorized transport systems. Beyond

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protecting components, pre-charge enhances safety by minimizing arc flash risks and preventing short circuits that could trigger relays or contactors unnecessarily. By controlling the inrush current, the system ensures reliable operation during repetitive start-up cycles, reduces the probability of component failure, and maintains operational integrity even under high-voltage conditions. Overall, this proposed method provides a robust, scalable solution for high-voltage power systems, combining controlled pre-charge functionality with SRAM-based control for precise, safe, and efficient device initialization.

V RESULTS & ANALYSIS

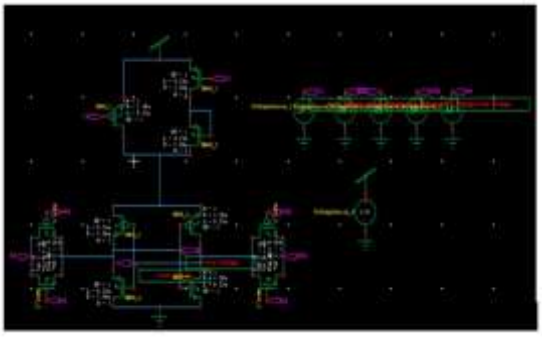

Fig.3 Proposed method schematic

This diagram shows a CMOS SRAM cell simulation schematic implemented using NMOS and PMOS transistors with supply voltage sources and control signals. The cross-coupled transistors store data (Q and QB), while word lines and bit lines control read and write operations during simulation**.** Two new SRAM cells: 11T-1 and 11T-2Completely half-select free operation Power-cutoff with floating-avoidance assist. This technique we are going to implement IIT SRAM with low power pre chargeable technique to improve the performance in SRAM with low power & compared to existing method.

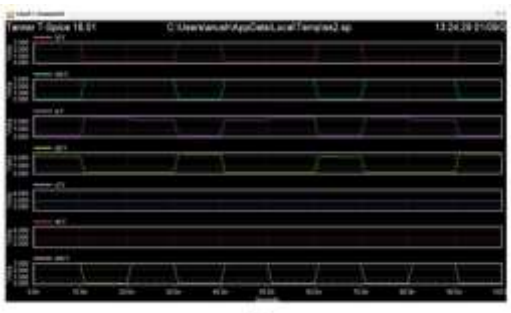

Fig.4 Proposed simulation results

The BL and BLB waveforms switch alternately, enabling correct write and read operations, while Q and QB change in a complementary manner, confirming proper data storage in the SRAM cell.The stable word line (WL/SL) control with clean transitions shows no read or write disturb, indicating reliable and low-leakage operation of the 11T SRAM.

```
Device and node counts:
            MOSFETs -      11
   MOSFET geometries -      2
     Voltage sources -      4
         Subcircuits -      0
   Model Definitions -      2
     Computed Models -      2
   Independent nodes -      9
      Boundary nodes -      5
         Total nodes -      14
```

Fig.5 Value Area

The device summary shows the proposed SRAM cell uses 11 MOSFETs with a limited number of nodes, indicating compact area overhead compared to conventional designs**.**

```
Parsing                 0.06 seconds
Setup                   0.05 seconds
DC operating point      0.06 seconds
Transient Analysis      0.01 seconds
Overhead                0.97 seconds
-------------------------------------
Total                   1.15 seconds
```

Fig.6 Delay

```
VVoltageSource_2 from time 0 to 100
Average power consumed -> 1.440304e-015 watts
Max power 2.727941e-004 at time 6.08697e-008
Min power 0.000000e+000 at time 0
```

Fig.7 Power

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VI CONCLUSION

This study presents two novel 11T SRAM cell topologies, 11T-1 and 11T-2, designed to be fully half-select-free and highly reliable, making them ideal for bit-interleaved memory architectures. By integrating power-cutoff techniques and simple write-'0'/write-'1' strategies, the proposed cells effectively eliminate both read disturb and write half-select disturb, while improving write-ability compared to conventional 6T cells. The results demonstrate enhanced read and write yield, confirming the robustness of these designs under low-voltage operation.A significant advantage of the proposed cells is the complete elimination of floating node issues, which were present in earlier power-cutoff SRAM designs. This ensures stable operation without auxiliary read or write assist circuits, reducing design complexity and improving energy efficiency. Using predictive 32 nm high-k metal gate CMOS technology, the impact of Bias Temperature Instability (BTI) on SRAM performance was analyzed. While all cells experience some reduction in Read Static Noise Margin (RSNM) under static stress, the 11T-1 and 11T-2 cells show enhanced RSNM resilience due to their inherent BTI tolerance.Although the designs introduce a slight increase in write delay, they maintain read delay and power consumption, while reducing both write power and leakage, and improving write margin (WM). Monte Carlo simulations and BTI analyses confirm that these cells are robust against process variations and transistor aging, making them highly suitable for reliable, low-power nanoscale SRAM applications. Overall, the proposed 11T SRAM cells provide a balanced solution for achieving high stability, energy efficiency, and long-term reliability in modern memory systems.

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