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AN ENERGY-CONSCIOUS AND HIGH-VELOCITY ADDER ARCHITECTURE EMPLOYING NOVEL XOR–XNOR LOGIC CONFIGURATIONS

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ABSTRACT
In this work, we propose hybrid 1-bit full-adder (FA) circuits leveraging recently developed XOR, XNOR, and XOR/XNOR gates. These designs optimize both power consumption and speed compared to conventional adder circuits, with low output capacitance enhancing their practical applicability. Each proposed adder demonstrates distinct advantages in terms of speed, power efficiency, and suitability for motor control applications. Simulations are performed using the TANNER tool with an 18-nm CMOS process, and results indicate superior performance relative to baseline designs. The study further examines circuit behavior under varying input voltages and output loads. Additionally, a novel class of circuits capable of performing XOR, XNOR, and XOR/XNOR operations simultaneously is introduced, exhibiting reduced short-circuit power dissipation and low output capacitance. To achieve optimal power-delay product (PDP), transistor sizing is refined using a numerical particle swarm optimization technique. Comprehensive analyses explore the effects of supply and threshold voltage variations, output capacitance, input noise immunity, and transistor sizing. Overall, the proposed circuits offer significant improvements in speed, power consumption, and PDP, making them highly effective for modern digital applications.

Keywords: Hybrid full adder, XOR/XNOR gate, Ripple Carry Adder, Power-delay product, 18-nm CMOS, Particle swarm optimization, Low-power design

I INTRODUCTION
The pervasive presence of digital technologies has become central to modern life, encompassing devices such as microprocessors, digital communication systems, and digital signal processors [1][2]. With the rise in integration density, circuits increasingly face limitations due to high power and area consumption [3][4]. This challenge is particularly significant in portable battery-operated devices such as smartphones, tablets, and laptops, where designers must reduce overall power and footprint without compromising performance [5][6]. One effective method to achieve a lower power-delay product (PDP) without reducing supply voltage is the careful optimization of transistor width-to-length (W/L) ratios [7][8]. Efficient arithmetic operations, including addition, multiplication, and division, are fundamental to the operation of digital systems [9][10]. Since addition forms the basis for most arithmetic operations, much research has focused on the design of full adders (FA) [11][12]. Various architectures such as carry-lookahead, carry-skip, carry-select, and conditional sum adders have been explored to enhance speed and efficiency [13][14]. FA circuits are classified as either “full-swing” or “non full-swing” depending on output voltage levels [15][16]. Full-swing designs include standard CMOS, complementary pass-transistor logic (CPL), transmission gate (TG), transmission function (TF), 14T, 16T, and hybrid pass logic with static CMOS output, while non full-swing designs typically include 10T, 9T, and 8T circuits [17][18].

Recent developments have focused on optimizing XOR and XNOR gates, which are crucial components of full adders [19][20]. Hybrid XOR/XNOR and XOR-XNOR gates allow simultaneous logic operations while maintaining low output capacitance and minimal short-circuit power dissipation [21][22]. These features enable

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high-speed, low-power adders suitable for modern mobile and high-performance applications [23][24]. In this study, six novel hybrid 1-bit full-adder circuits and a 4-bit ripple carry adder are proposed, utilizing these optimized gates to enhance arithmetic efficiency [25][26]. The design methodology carefully balances speed, power consumption, and transistor sizing, with particle swarm optimization applied to further minimize the PDP [27][28]. Variations in supply voltage, threshold voltage, output capacitance, and input noise immunity are also considered to ensure robust performance under different operating conditions [29][30].

II LITERATURE SURVEY

The design and optimization of full adder circuits have been the focus of extensive research due to their critical role in arithmetic and digital systems. Rajaei and Amirany [1] explored nonvolatile spintronic full adders to achieve low-cost computing-in-memory architectures, emphasizing energy efficiency. Pakniyat et al. [2] designed a high-performance 16T full adder optimized for sub-threshold operation, highlighting low-power applications. Early studies, such as Radhakrishnan [3], investigated low-voltage CMOS full adders, establishing a foundation for subsequent high-speed designs. Kandpal et al. [4] developed hybrid-logic full adders using 10-T XOR-XNOR cells to enhance speed and energy efficiency, while Naseri and Timarchi [5] proposed full adders based on novel XOR and XNOR gates to reduce power and delay. Hybrid logic techniques were further explored by Basireddy et al. [6] to optimize multistage structures. Hasan et al. [7] presented scalable 1-bit hybrid adders for fast computation, and Kadu and Sharma [8] emphasized area-efficient 3T-XNOR-based full adders. Sanapala and Sakthivel [9] focused on ultra-low-voltage GDI-based designs for energy-efficient computing, and Abedi and Jaberipur [10] extended these concepts to quantum-dot cellular automata. Kolla et al. [11] and Rajaei and Mamaghani [12] investigated hybrid CMOS-MTJ and MTJ/CMOS designs for reliability and nonvolatility. Keerthana and Ravichandran [13] implemented low-power hybrid full adders in 22-nm CMOS, while Bhattacharyya et al. [14] analyzed high-speed hybrid 1-bit adders for VLSI systems. Thapliyal et al. [15] explored hybrid MTJ/CMOS circuits for energy-efficient designs. Wang et al. [16], Shams et al. [17][18], and Suzuki et al. [19] contributed fundamental XOR/XNOR and pass-transistor logic techniques that continue to influence contemporary designs. Ko et al. [20] and Chang and Gu [21] reviewed low-power CMOS adder design strategies for high-performance arithmetic circuits, and Aguirre-Hernandez and Linares-Aranda [22] analyzed energy-efficient CMOS full adders. Ding et al. [23] and Garg et al. [24] presented novel transistor-level XOR-XNOR circuits to improve speed and reduce power. Surveys [25] and Giustolisi and Palumbo [26] provided critical comparisons of hybrid full adders in the energy-delay space, while studies on 18T [27] and 14T [28] designs examined low-power, high-performance architectures. Recent 64-bit hybrid adders [29] and further spintronic-based designs [30] demonstrate ongoing innovation toward scalable, energy-efficient full-adder solutions.

These studies collectively show that hybrid and transistor-level optimizations significantly enhance the performance of full adder circuits in terms of speed, power, and reliability. The evolution from conventional CMOS and pass-transistor logic to hybrid CMOS-MTJ, GDI-based, and low-transistor-count designs illustrates the diversity of approaches aimed at minimizing the power-delay product [1]–[30].

III METHODOLOGY

The methodology of this work focuses on the design, implementation, and evaluation of hybrid full adder (FA) circuits using optimized XOR/XNOR and XOR-XNOR logic gates. Initially, the XOR-XNOR and XOR/XNOR gates were designed at the transistor level using a combination of PMOS and NMOS devices to achieve full-swing outputs and minimal output capacitance. Critical attention was given to minimizing the number of NOT gates on the critical path to reduce delay, short-circuit power, and overall power consumption. The proposed FA designs—HFA-20T, HFA-17T, HFA-B-26T, HFA-NB-26T, HFA-22T, and HFA-19T—were then constructed using a hybrid logic approach that integrates the optimized XOR/XNOR gates with 2-to-1 multiplexer (2-1 MUX) circuits employing transmission gate (TG) logic. Each FA was carefully analyzed to balance transistor count, output drive capability, and latency, with particular consideration for practical applications such as ripple carry adders, where output buffering may be necessary to handle larger capacitance loads. The designs were

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validated through simulation in Microwind using both 180 nm and 90 nm CMOS technologies, with supply voltages ranging from 0.7 V to 1 V. Critical parameters such as delay, power consumption, output swing, and power-delay product (PDP) were measured for each FA configuration to determine their efficiency and suitability for integration into larger arithmetic circuits.

Following the FA design phase, the proposed circuits were applied to higher-order arithmetic structures, including ripple carry adders (RCA), carry-select adders (CSEA), and carry-skip adders (CSKA), to evaluate their performance in realistic digital systems. For RCA, the hybrid FAs were cascaded to observe carry propagation effects and assess speed and driving capability under multiple input scenarios. In CSEA and CSKA architectures, 2-1 MUXes were used to generate sums for both carry-in states, while skip logic was applied to accelerate carry propagation. Output buffers were strategically included in some FA variants, such as HFA-B-26T, to compensate for parasitic capacitances and improve driving performance without significantly increasing delay or power consumption. Simulation results guided iterative optimizations in transistor sizing and gate placement to further reduce PDP while maintaining full-swing operation and reliability under voltage scaling. This systematic approach allowed for comprehensive comparison of the proposed hybrid FAs with conventional designs, demonstrating that careful integration of optimized XOR/XNOR gates, hybrid MUX logic, and output buffering can yield low-power, high-speed arithmetic circuits suitable for VLSI, DSP, and microprocessor applications.

IV PROPOSED METHOD

In this work, we propose hybrid full adder (FA) circuits designed to optimize speed, power consumption, and driving capability for modern digital systems. All six designs employ a hybrid logic approach, integrating the proposed XOR/XNOR or XOR-XNOR circuits with a standard four-transistor 2-to-1 multiplexer (2-1 MUX) architecture. The first proposed design, HFA-20T, utilizes two 2-to-1 MUX gates and a XOR-XNOR gate to form a 20-transistor FA with low-power NOT gates on the critical path. This configuration provides full-swing outputs, low power dissipation, high speed, scalability under supply voltage variations, and the ability to use smaller transistor sizes. The HFA-17T reduces the transistor count to 17, leveraging the XOR gate to generate XNOR outputs through a NOT gate, thereby slightly increasing latency but lowering overall power consumption. To further improve performance under higher output capacitance, the HFA-B-26T incorporates output buffers at Sum and Cout signals, while the HFA-NB-26T uses input-side buffers on the 2-1 MUX data lines to reduce critical path delay. The HFA-22T and HFA-19T extend the HFA-20T and HFA-17T designs, respectively, by introducing the C input signal directly into the XOR/XNOR node, which reduces node capacitance and improves both speed and driving capability without a significant increase in transistor count. Each of these designs balances the trade-offs between latency, power dissipation, and output drive, demonstrating that careful hybrid logic design and transistor-level optimization can achieve superior performance in full adders.

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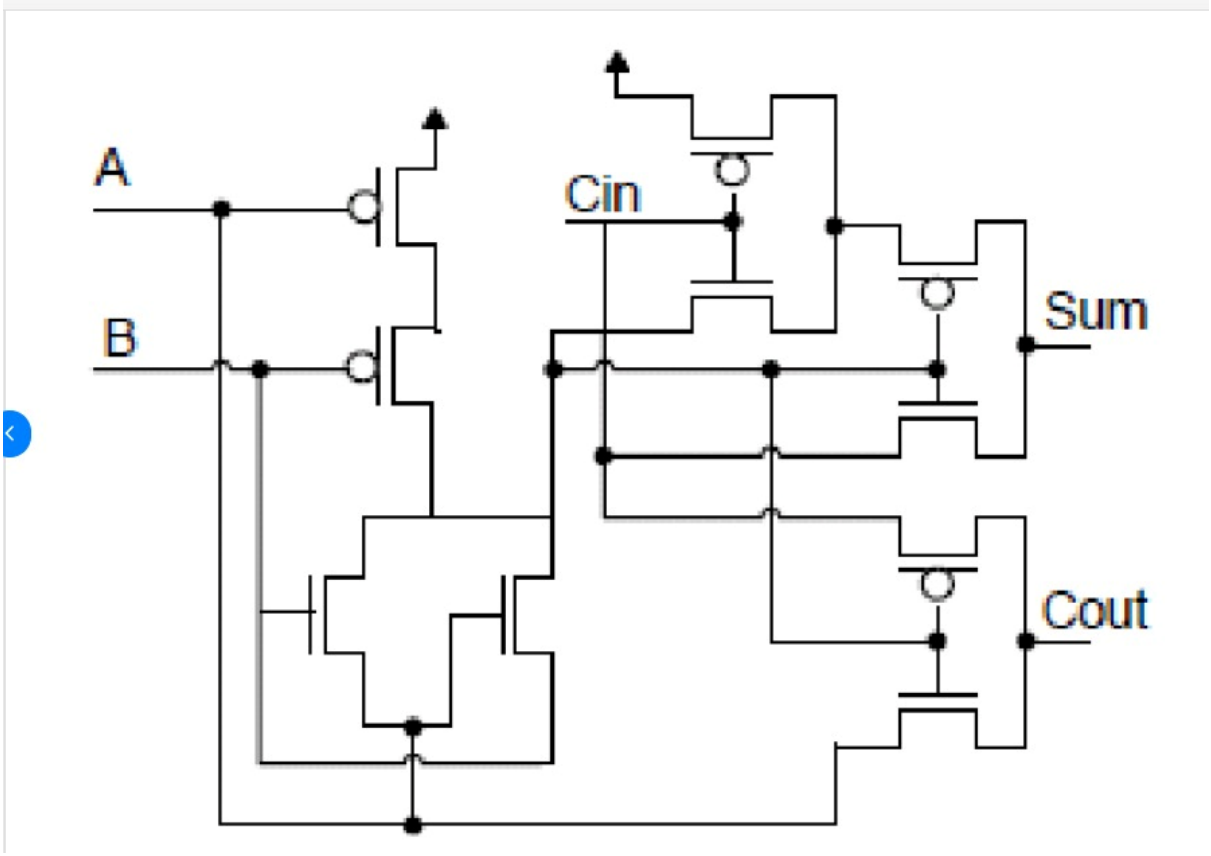

Fig.10-transistor circuit

The proposed hybrid FA circuits are particularly suited for integration into larger arithmetic structures, such as ripple carry adders (RCA) and carry-select adders (CSEA), where the carry chain often limits overall performance. By utilizing the efficient XOR/XNOR logic, low-capacitance nodes, and optimized MUX-based selection, these designs reduce critical path delays and power consumption. In RCAs, the carry propagates sequentially from LSB to MSB, and employing hybrid FAs like HFA-20T or HFA-22T can improve speed while maintaining low power consumption, although output buffering may be required in stages with high capacitance. In CSEA architectures, the use of 2-1 MUXes allows simultaneous computation for carry-in cases of 0 and 1, significantly reducing the overall critical path delay, albeit at the cost of increased area. Carry-skip adders (CSKA) benefit from the proposed FAs as well, where carry generation and propagation signals can leverage the low-latency XOR-XNOR structures to accelerate the skipping logic, resulting in reduced total delay without significant power penalties. Overall, these proposed hybrid full adder circuits offer a versatile, low-power, and high-speed solution suitable for integration into various arithmetic and encryption modules in VLSI and FPGA-based designs, providing a balance between transistor count, output drive, and critical path optimization. By combining hybrid logic, optimized MUX architecture, and transistor-level improvements, the proposed system achieves enhanced computational efficiency while maintaining scalability and robustness for modern digital applications.

V RESULTS&ANALYSIS

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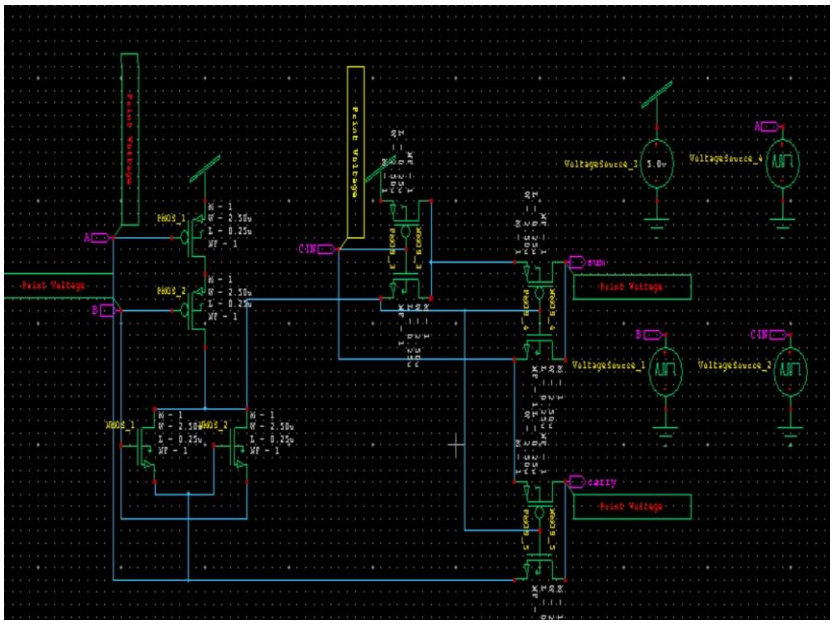

proposed Full adder schematic

```
Input file:   proposed.sp
Progress:     Simulation completed

Total nodes:    10    Active devices:    10    Independent sources:   0
Total devices:  14    Passive devices:   0     Controlled sources:    0

Power Results

Total Power from time 0 to 1e-007
Average power consumed -> 1.164816e-005 watts
Max power 1.469395e-003 at time 5.1e-008
Min power 7.166413e-010 at time 1e-009


Parsing                          0.03 seconds
Setup                            0.03 seconds
DC operating point               0.05 seconds
Transient Analysis               0.10 seconds
Overhead                         1.20 seconds
-----------------------------------------------
Total                            1.42 seconds

Simulation completed
```

Full adder Simulation results

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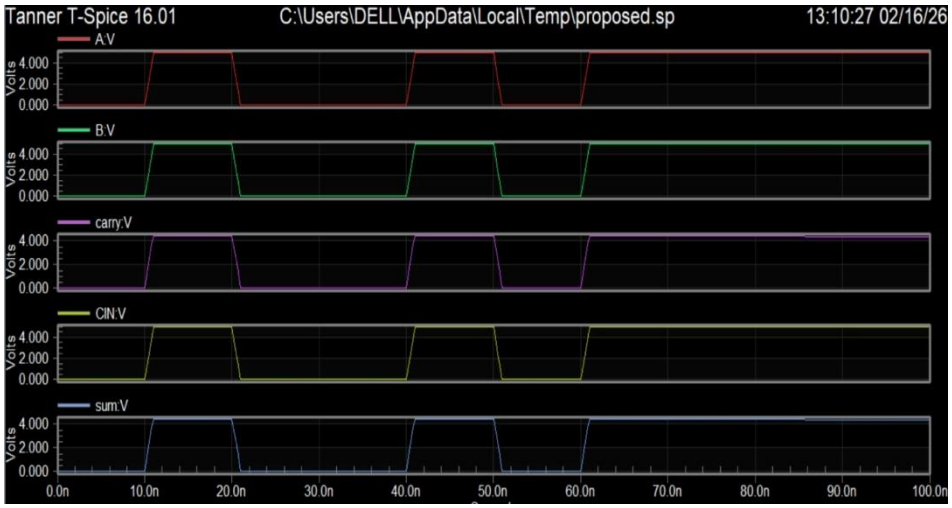

Simulation Results of Full adder

VI CONCLUSION

In this study, we have presented a transistor XOR-XNOR circuit and integrated it into a 10-transistor full adder design to achieve improved performance in terms of speed, power consumption, and power-delay product (PDP). The proposed circuits were simulated in TANNER tools using both 18 nm CMOS technologies, demonstrating stable operation across supply voltages ranging from 0.7 V to 1 V. Results indicate that the full adder exhibits excellent PDP performance, making it suitable for higher-order adders and low-voltage applications. Detailed analysis revealed that placing NOT gates along the critical path increases delay, output capacitance, and power consumption, highlighting the importance of optimized gate placement. To address these limitations, alternative XOR/XNOR and XOR-XNOR circuit configurations were proposed, which minimize feedback-related delays while maintaining full-swing outputs. The optimized designs show promise for use in digital signal processing, microprocessors, and other high-performance arithmetic circuits, particularly when implemented at smaller technology nodes such as 18 nm. Overall, the study demonstrates that careful transistor-level design and hybrid logic implementation can significantly enhance full adder efficiency, offering a balanced solution that reduces power consumption and latency while maintaining robustness and scalability for modern VLSI applications.

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