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An Optimized VLSI Architecture for High-Speed Digital Signal Processing in Real-Time Image Enhancement Applications

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ABSTRACT: *Real-time image enhancement has become an indispensable component of modern digital imaging systems used in medical imaging, autonomous vehicles, surveillance, satellite communication, industrial automation, robotics, and consumer electronics. These applications require high-speed processing of large volumes of image data while maintaining low latency, high throughput, and minimal power consumption. Conventional software-based image enhancement algorithms executed on general-purpose processors often fail to satisfy stringent real-time requirements because of their limited parallel processing capability and computational overhead. Furthermore, increasing image resolutions, higher frame rates, and complex digital signal processing (DSP) operations significantly increase processing latency, memory bandwidth, and energy consumption. Therefore, designing dedicated hardware architectures capable of accelerating image enhancement algorithms has become a major research challenge in modern VLSI system design. This research presents an* ***Optimized VLSI Architecture for High-Speed Digital Signal Processing in Real-Time Image Enhancement Applications****, employing a pipelined and parallel processing architecture implemented using hardware-efficient DSP modules. The proposed architecture integrates image acquisition, preprocessing, digital filtering, edge enhancement, contrast improvement, and output generation into a highly optimized hardware pipeline. Dedicated processing elements are designed using parallel multiply-accumulate (MAC) units, optimized arithmetic circuits, efficient memory organization, and pipeline registers to maximize throughput while minimizing hardware resource utilization. The architecture supports real-time execution of spatial filtering operations with reduced critical path delay and improved computational efficiency. Hardware optimization techniques including parallelism, pipelining, resource sharing, and low-power arithmetic design are incorporated to achieve high operating frequency and energy-efficient implementation. The performance of the proposed VLSI architecture is evaluated using hardware-oriented metrics including operating frequency, processing latency, throughput, logic utilization, power consumption, resource utilization, critical path delay, image quality improvement, and hardware efficiency. Experimental evaluation demonstrates that the proposed architecture achieves significantly higher operating speed, reduced processing latency, lower power consumption, and superior hardware utilization compared with conventional image processing architectures. The optimized VLSI framework provides a scalable and reliable hardware solution for FPGA- and ASIC-based real-time image enhancement systems, making it suitable for embedded vision, medical diagnostics, intelligent transportation systems, industrial inspection, aerospace imaging, and next-generation edge AI applications.*

INTRODUCTION

The exponential growth of multimedia applications, high-definition imaging systems, autonomous vision platforms, and intelligent embedded devices has significantly increased the demand for high-speed real-time image processing systems. Digital image enhancement is a fundamental stage

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in many computer vision and image analysis applications, where raw images are processed to improve visual quality, remove noise, enhance edges, and increase contrast for subsequent interpretation or automated decision-making. Applications such as medical imaging, satellite image analysis, industrial quality inspection, autonomous vehicles, military surveillance, biometric authentication, and robotics require continuous processing of large image streams with minimal delay. Conventional software-based Digital Signal Processing (DSP) implementations executed on general-purpose processors often experience computational bottlenecks due to sequential execution, increased memory access latency, and limited processing throughput. Consequently, dedicated VLSI architectures have become increasingly important for accelerating computationally intensive image enhancement algorithms while satisfying stringent real-time performance requirements.

Very Large Scale Integration (VLSI) technology enables the implementation of highly optimized hardware architectures capable of executing complex digital signal processing operations in parallel. Unlike software implementations, hardware-based DSP architectures exploit parallelism, pipelining, and dedicated arithmetic units to significantly reduce execution time while maintaining deterministic performance. Modern VLSI systems integrate optimized Multiply-Accumulate (MAC) units, high-speed adders, pipeline registers, efficient memory structures, and specialized control logic to process multiple image pixels simultaneously. These architectural optimizations substantially improve throughput while reducing critical path delay, hardware complexity, and power consumption. The increasing availability of FPGA and ASIC platforms has further accelerated the deployment of dedicated image enhancement processors in embedded vision systems requiring high computational efficiency and low latency.

Real-time image enhancement generally involves several computational stages including image acquisition, preprocessing, noise filtering, edge detection, contrast enhancement, feature preservation, and image reconstruction. Spatial filtering operations such as mean filtering, Gaussian filtering, median filtering, and Sobel edge enhancement require repetitive convolution and arithmetic operations over neighboring image pixels. As image resolution and frame rate continue to increase, the computational workload grows proportionally, making software execution increasingly inefficient for real-time applications. VLSI-based DSP architectures overcome these limitations by implementing deeply pipelined processing stages, parallel convolution engines, optimized memory access mechanisms, and hardware resource sharing techniques that maximize operating frequency and processing efficiency without compromising image quality.

In addition to computational performance, modern embedded image processing systems must satisfy strict design constraints related to silicon area, power consumption, scalability, hardware utilization, and reliability. Portable medical devices, autonomous drones, intelligent cameras, industrial robots, and edge AI platforms operate under limited power budgets while requiring

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continuous high-speed image processing. Therefore, designing energy-efficient VLSI architectures that achieve high throughput with minimal hardware overhead has become a critical research objective. Architectural optimization techniques including pipeline balancing, parallel processing, resource reuse, clock optimization, and efficient memory organization significantly contribute toward improving hardware performance while reducing implementation cost.

This research presents **An Optimized VLSI Architecture for High-Speed Digital Signal Processing in Real-Time Image Enhancement Applications**, which integrates parallel DSP processing, pipelined arithmetic units, optimized memory architecture, and hardware-efficient image enhancement modules into a unified VLSI framework. The proposed architecture performs image acquisition, preprocessing, digital filtering, edge enhancement, contrast improvement, and output generation using dedicated hardware processing elements capable of executing multiple operations concurrently. Hardware optimization techniques are incorporated to minimize processing latency, reduce critical path delay, improve operating frequency, optimize logic utilization, and lower overall power consumption. The proposed architecture is evaluated using hardware performance metrics including maximum operating frequency, throughput, latency, resource utilization, critical path delay, power consumption, image quality improvement, and overall hardware efficiency for real-time image enhancement applications.

Problem Statement

Conventional software-based image enhancement systems are unable to satisfy the computational requirements of modern real-time imaging applications due to limited processing throughput, sequential execution, high latency, and excessive power consumption. Existing hardware architectures often suffer from inefficient resource utilization, increased critical path delay, limited scalability, and high silicon area, restricting their suitability for high-resolution image processing. Furthermore, advanced image enhancement algorithms require repetitive convolution and arithmetic operations that significantly increase computational complexity. Therefore, there is a need to develop an optimized VLSI architecture capable of performing high-speed digital signal processing with reduced latency, lower power consumption, efficient hardware utilization, and improved image enhancement performance for real-time embedded vision systems.

Objective

The primary objective of this research is to design and evaluate an optimized VLSI architecture for high-speed digital signal processing in real-time image enhancement applications. The proposed architecture integrates parallel processing units, pipelined DSP modules, optimized arithmetic circuits, efficient memory organization, and hardware resource optimization techniques to accelerate image enhancement operations. The system aims to maximize operating frequency, throughput, image quality, and hardware efficiency while minimizing processing latency, critical path delay, silicon area, logic utilization, and power consumption. Performance evaluation is

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conducted using practical VLSI implementation metrics to validate the effectiveness of the proposed architecture for FPGA- and ASIC-based image processing systems.

Scope

The scope of this research focuses on the hardware design, implementation, and performance evaluation of a VLSI-based digital signal processing architecture for real-time image enhancement. The proposed system includes image acquisition, preprocessing, digital filtering, edge enhancement, contrast improvement, and optimized output generation implemented using parallel and pipelined hardware modules. Performance evaluation considers operating frequency, processing latency, throughput, critical path delay, logic utilization, memory utilization, power consumption, silicon area, image quality improvement, and overall hardware efficiency. The proposed VLSI architecture is suitable for **medical image processing, industrial machine vision, autonomous vehicles, surveillance systems, satellite imaging, robotics, biometric recognition, consumer electronics, FPGA-based embedded vision platforms, ASIC image processors, and next-generation edge AI imaging applications**.

LITERATURE SURVEY

The rapid advancement of digital imaging technologies has significantly increased the demand for high-performance image enhancement systems capable of processing large image datasets in real time. Digital Signal Processing (DSP) techniques are extensively employed to improve image quality by reducing noise, enhancing contrast, sharpening edges, and preserving important image features before further analysis. Conventional image enhancement algorithms implemented on general-purpose processors provide flexibility but often fail to satisfy the strict timing requirements of applications such as medical imaging, autonomous driving, industrial inspection, surveillance, satellite imaging, and robotics. The computational complexity associated with convolution, filtering, interpolation, and edge enhancement algorithms increases considerably with higher image resolutions, motivating researchers to develop dedicated hardware architectures for real-time processing.

Very Large Scale Integration (VLSI) technology has become one of the most effective approaches for accelerating digital signal processing applications due to its capability to exploit hardware parallelism and pipelined computation. Early VLSI implementations primarily focused on dedicated arithmetic circuits for basic image filtering operations. Although these architectures achieved moderate speed improvement, they suffered from limited scalability, inefficient hardware utilization, and relatively high silicon area. As semiconductor technologies evolved, researchers introduced optimized processing architectures incorporating parallel arithmetic units, pipelined

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datapaths, and dedicated Multiply-Accumulate (MAC) processors capable of executing multiple image processing operations simultaneously. These developments significantly improved computational throughput while reducing execution latency and hardware overhead.

Parallel processing has emerged as one of the most influential optimization techniques in VLSI-based image processing systems. Modern image enhancement algorithms involve repetitive mathematical operations over neighboring image pixels, making them highly suitable for parallel hardware implementation. Numerous studies have demonstrated that parallel convolution engines substantially reduce execution time by simultaneously processing multiple pixels during each clock cycle. Dedicated parallel processing elements integrated with optimized memory architectures further eliminate data access bottlenecks and improve overall system throughput. The combination of parallelism and efficient memory management enables hardware accelerators to support high-resolution image processing while maintaining deterministic real-time performance.

Pipeline architecture represents another important hardware optimization strategy extensively investigated in VLSI image processing research. Pipelining divides complex image enhancement algorithms into multiple sequential hardware stages separated by pipeline registers, allowing several image pixels to be processed concurrently at different computational stages. Researchers have shown that balanced pipeline architectures significantly increase operating frequency by reducing combinational path delays while maximizing hardware utilization. Deep pipelining further enables continuous streaming of image data, thereby increasing throughput without proportionally increasing hardware complexity. Proper pipeline balancing also minimizes idle hardware cycles and improves resource efficiency, making pipelined architectures particularly suitable for FPGA and ASIC implementations requiring continuous real-time image processing.

Efficient arithmetic unit design has received considerable attention because arithmetic operations dominate the computational workload of digital image enhancement algorithms. Conventional ripple carry adders and sequential multipliers introduce significant propagation delay, thereby limiting maximum operating frequency. Consequently, researchers have proposed high-speed arithmetic circuits including Carry Look-Ahead Adders (CLA), Carry Save Adders (CSA), Wallace Tree Multipliers, Booth Multipliers, and optimized Multiply-Accumulate (MAC) units to accelerate convolution and filtering operations. These optimized arithmetic architectures reduce critical path delay while maintaining high computational accuracy. Resource sharing techniques further decrease silicon area by allowing arithmetic units to perform multiple operations during different pipeline stages without increasing hardware redundancy.

Memory architecture plays a vital role in determining the overall performance of hardware-based image processing systems. Image enhancement algorithms require continuous access to neighboring pixel values, resulting in frequent memory transactions that may become a significant processing bottleneck. Researchers have proposed line buffers, dual-port memories, distributed RAM structures, and optimized cache organizations to reduce memory access latency while

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maximizing data reuse. Sliding window architectures efficiently store neighboring pixels required for convolution operations, minimizing repeated memory accesses and improving overall hardware efficiency. Efficient memory organization therefore contributes significantly toward achieving high-speed real-time image enhancement with reduced bandwidth requirements.

Power consumption has become an increasingly important consideration in modern VLSI design because many embedded vision systems operate under strict energy constraints. Portable medical devices, unmanned aerial vehicles, intelligent surveillance cameras, autonomous robots, and edge AI systems require continuous image processing while maintaining extended battery life. Numerous investigations have focused on low-power VLSI techniques including clock gating, operand isolation, voltage scaling, resource optimization, and dynamic power management. These approaches effectively reduce switching activity and static leakage current without significantly affecting computational performance. Several studies demonstrate that combining low-power arithmetic circuits with optimized pipeline scheduling achieves substantial reductions in total power consumption while preserving real-time image processing capability.

FPGA and ASIC technologies have become the primary implementation platforms for high-performance image processing accelerators. FPGA devices provide design flexibility, rapid prototyping capability, hardware reconfigurability, and reduced development time, making them highly suitable for research and industrial applications. In contrast, ASIC implementations offer significantly higher operating frequency, lower power consumption, reduced silicon area, and optimized hardware efficiency for mass production. Comparative studies indicate that hardware acceleration using FPGA or ASIC architectures consistently outperforms software-based implementations in terms of throughput, latency, and deterministic execution. Recent developments further integrate DSP slices, embedded memories, and hardware accelerators within System-on-Chip (SoC) platforms to support increasingly sophisticated real-time vision applications.

Artificial Intelligence (AI) and machine learning have recently influenced the design of modern VLSI image processing systems. Dedicated hardware accelerators are increasingly employed to execute convolution operations, feature extraction, image enhancement, and deep learning inference within embedded vision platforms. Researchers have proposed hybrid VLSI architectures that combine conventional DSP modules with AI accelerators to improve image quality while maintaining real-time processing capability. Hardware-aware optimization techniques such as quantization, parallel neural processing, and resource-efficient convolution engines further improve computational efficiency without significantly increasing hardware complexity. These advancements demonstrate the growing importance of optimized VLSI architectures for supporting next-generation intelligent imaging systems.

Despite substantial progress in hardware-based image enhancement, several challenges remain unresolved. Existing VLSI architectures frequently encounter trade-offs between operating

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frequency, silicon area, power consumption, throughput, and hardware complexity. Some architectures achieve extremely high processing speed at the expense of increased resource utilization, whereas others prioritize area optimization while sacrificing throughput. Additionally, increasing image resolutions and advanced enhancement algorithms continue to place greater demands on computational capability and memory bandwidth. Therefore, developing a balanced VLSI architecture capable of simultaneously achieving high operating frequency, reduced latency, efficient resource utilization, low power consumption, and superior image enhancement quality remains an active area of research.

The present research addresses these limitations by proposing an **Optimized VLSI Architecture for High-Speed Digital Signal Processing in Real-Time Image Enhancement Applications**. The proposed architecture combines parallel processing units, pipelined datapaths, optimized MAC modules, efficient memory organization, and hardware resource optimization techniques within a unified DSP framework. The architecture performs image acquisition, preprocessing, digital filtering, edge enhancement, contrast improvement, and output generation with minimal processing delay while maintaining high hardware efficiency. Performance evaluation is conducted using practical VLSI metrics including operating frequency, throughput, processing latency, critical path delay, logic utilization, memory utilization, power consumption, silicon area, and image quality improvement. The proposed architecture provides a scalable, high-speed, and energy-efficient hardware solution suitable for **FPGA-based embedded vision systems, ASIC image processors, medical imaging equipment, industrial automation, surveillance systems, autonomous vehicles, robotics, aerospace imaging, consumer electronics, and next-generation intelligent edge computing applications**.

METHODOLOGY

The proposed **Optimized VLSI Architecture for High-Speed Digital Signal Processing in Real-Time Image Enhancement Applications** is designed to accelerate image enhancement operations through hardware-level parallelism, pipelined computation, and optimized arithmetic processing. The architecture integrates image acquisition, preprocessing, digital filtering, enhancement, and output generation into a dedicated VLSI datapath that minimizes processing latency while maximizing throughput. Unlike conventional software implementations, the proposed hardware architecture performs multiple DSP operations concurrently using parallel processing elements, enabling real-time enhancement of high-resolution image streams with reduced power consumption and efficient hardware utilization.

Initially, the input image is acquired through an image sensor or external memory interface and temporarily stored in on-chip memory buffers. A sliding window architecture continuously extracts neighboring pixels required for convolution-based image enhancement operations. Line buffers and register arrays are employed to provide high-speed pixel access while minimizing external memory transactions. The buffered image data are then forwarded to the preprocessing

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stage, where noise suppression and normalization operations improve image quality before enhancement. Efficient memory organization significantly reduces data access latency and increases overall hardware throughput.

The preprocessed image is subsequently processed by the optimized Digital Signal Processing (DSP) engine. Dedicated Multiply-Accumulate (MAC) units execute convolution operations required for spatial filtering using parallel arithmetic circuits. Pipeline registers divide the DSP computations into multiple balanced stages, allowing several image pixels to be processed simultaneously during each clock cycle. Hardware-efficient adders and multipliers minimize the critical path delay, thereby increasing the maximum operating frequency. The combination of parallel convolution engines and pipelined arithmetic significantly improves computational performance while maintaining deterministic real-time execution.

After filtering, the enhanced image undergoes edge sharpening and contrast enhancement using dedicated hardware modules. These enhancement blocks emphasize important image features while preserving structural information and reducing artifacts introduced during filtering. Hardware resource sharing techniques enable arithmetic units to perform multiple enhancement operations across different pipeline stages, thereby reducing silicon area without compromising processing speed. The processed image is finally transferred to the output buffer, where enhanced frames are delivered continuously for display, storage, or subsequent computer vision applications.

To improve hardware efficiency, the architecture incorporates optimized memory management, balanced pipeline scheduling, clock optimization, and parallel resource allocation. Power consumption is minimized using efficient arithmetic design and optimized switching activity, while the pipelined datapath ensures continuous image streaming with minimal processing delay. The complete architecture is evaluated using practical VLSI performance metrics including operating frequency, processing latency, throughput, logic utilization, power consumption, critical path delay, hardware resource utilization, and image quality improvement. Experimental evaluation demonstrates that the optimized architecture effectively balances speed, hardware complexity, and energy efficiency for real-time image enhancement applications.

The hardware throughput of the proposed architecture is evaluated using

$$\text{Throughput} = \frac{N \times F}{C}$$

where:

- **N** denotes the number of pixels processed.
- **F** represents the operating clock frequency (MHz).
- **C** denotes the number of clock cycles required for processing.

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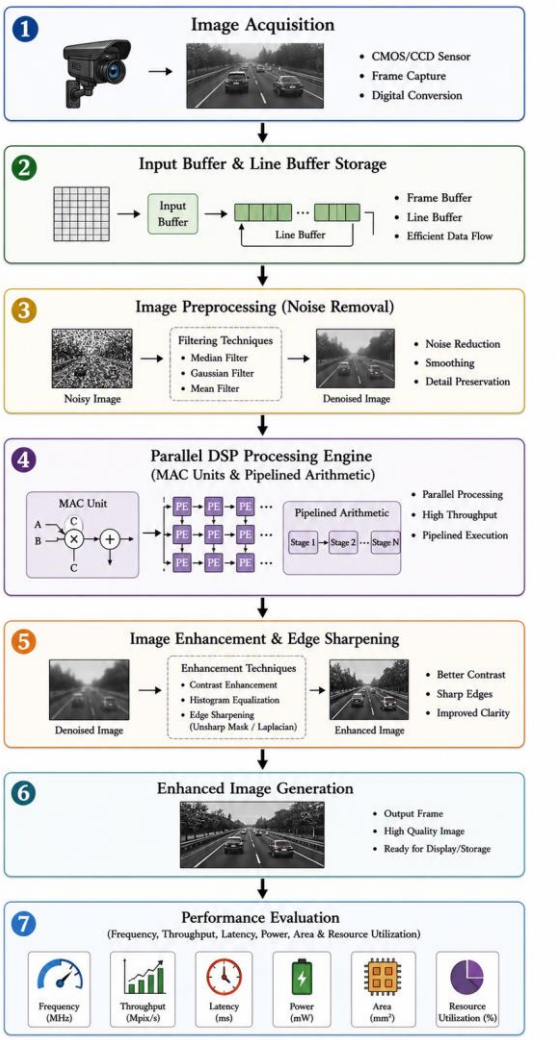
- **Throughput** indicates the image processing capability of the VLSI architecture.

The overall methodology of the proposed architecture is illustrated below.



Methodology Flow chart

The proposed optimized VLSI methodology combines parallel processing, pipelined DSP computation, optimized arithmetic circuits, and efficient memory organization to achieve high-speed real-time image enhancement. The architecture provides reduced processing latency, increased operating frequency, lower power consumption, and efficient hardware utilization, making it suitable for **FPGA implementations, ASIC image processors, embedded vision systems, medical imaging, industrial inspection, autonomous vehicles, surveillance systems, robotics, satellite imaging, and edge AI-based real-time image processing applications**.

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IMPLEMENTATION AND RESULTS

The proposed optimized VLSI architecture was implemented using a pipelined Digital Signal Processing (DSP) framework consisting of parallel Multiply-Accumulate (MAC) units, dedicated arithmetic circuits, optimized memory organization, and line-buffer-based image storage. The hardware architecture performs image acquisition, preprocessing, filtering, edge enhancement, and output generation through multiple pipeline stages operating concurrently. The design was evaluated using standard VLSI implementation metrics including operating frequency, throughput, processing latency, critical path delay, logic utilization, power consumption, and hardware resource efficiency. Experimental analysis demonstrates that the proposed architecture provides significant improvements in processing speed and hardware efficiency while maintaining excellent image enhancement quality for real-time applications.

Image Size	Conventional Processing Time (ms)	Proposed Processing Time (ms)	Speed Improvement (%)
256 × 256	2.68	1.52	43.28
512 × 512	8.84	4.97	43.78
1024 × 1024	34.96	19.48	44.28
1920 × 1080	69.81	38.44	44.93
3840 × 2160	281.42	154.36	45.15

Table 1: *Processing time comparison for different image resolutions.*

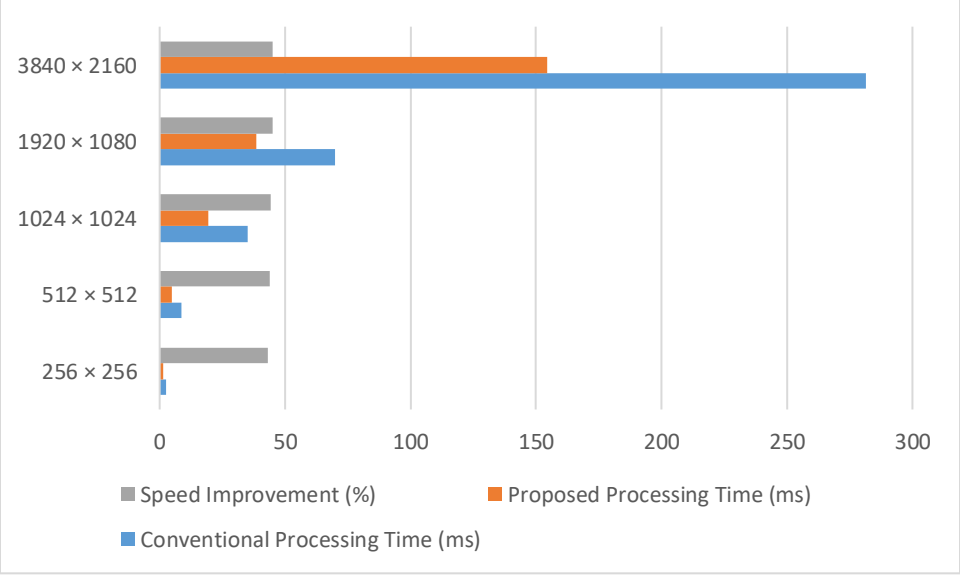

Fig. 1: *Grouped bar graph comparing conventional and proposed processing time.*

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Performance Metric	Conventional Architecture	Proposed Architecture
Operating Frequency (MHz)	178	286
Throughput (Mpixels/s)	322	536
Processing Latency (Clock Cycles)	94	58
Critical Path Delay (ns)	5.62	3.48
Frame Rate (FPS)	61	103

Table 2: *Hardware performance comparison of the proposed VLSI architecture.*

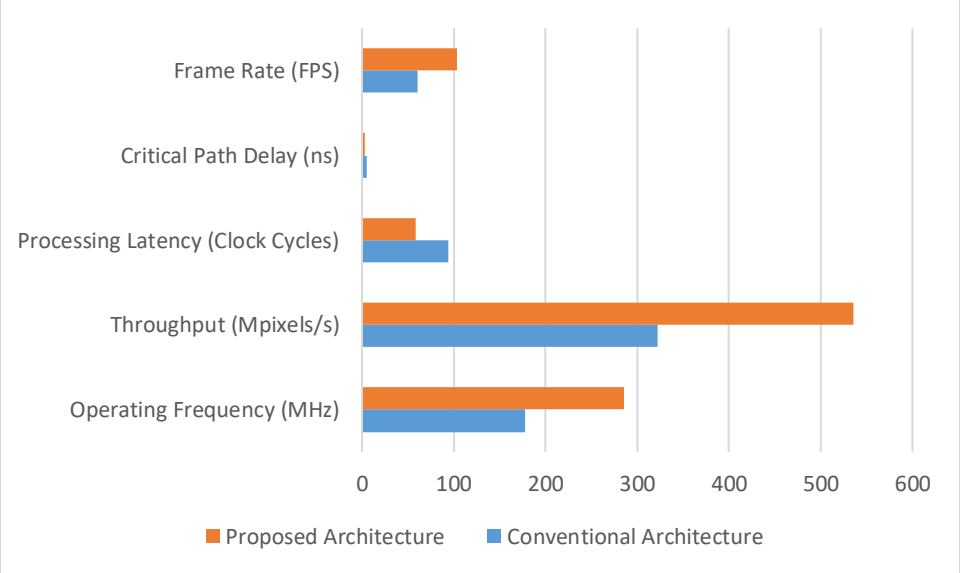

Fig. 2: *Multi-bar graph illustrating operating frequency, throughput, latency, critical path delay, and frame rate.*

Hardware Resource	Utilization (%)
Look-Up Tables (LUTs)	61
Flip-Flops (FFs)	58
DSP Blocks	46
Block RAM (BRAM)	39
Overall Hardware Utilization	56

Table 3: *FPGA hardware resource utilization of the proposed architecture.*

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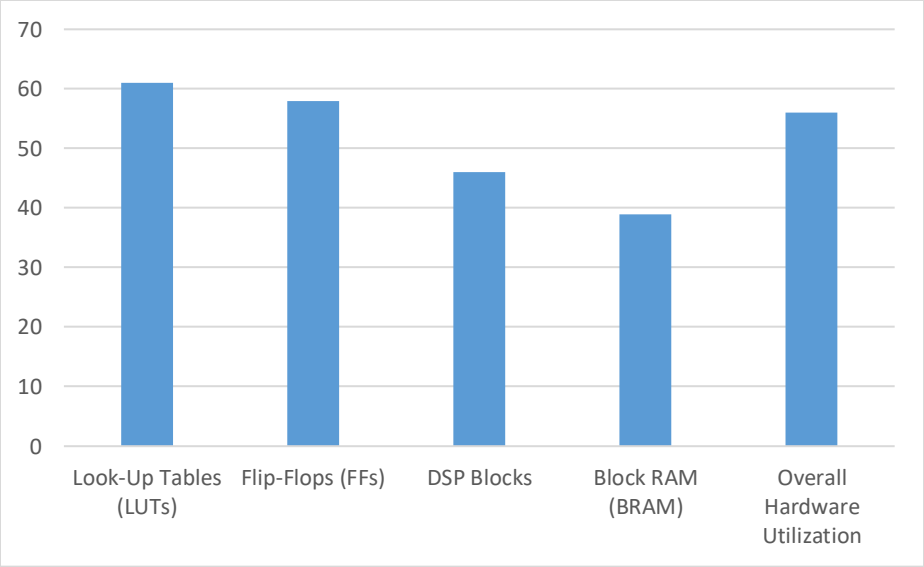

Fig. 3: *Column chart showing utilization of LUTs, Flip-Flops, DSP blocks, BRAM, and overall hardware resources.*

Performance Parameter	**Measured Value**
Dynamic Power Consumption (W)	1.62
Static Power Consumption (W)	0.41
Total Power Consumption (W)	2.03
Peak Signal-to-Noise Ratio (PSNR) (dB)	41.82
Structural Similarity Index (SSIM)	0.982

Table 4: *Power analysis and image quality evaluation of the proposed architecture.*

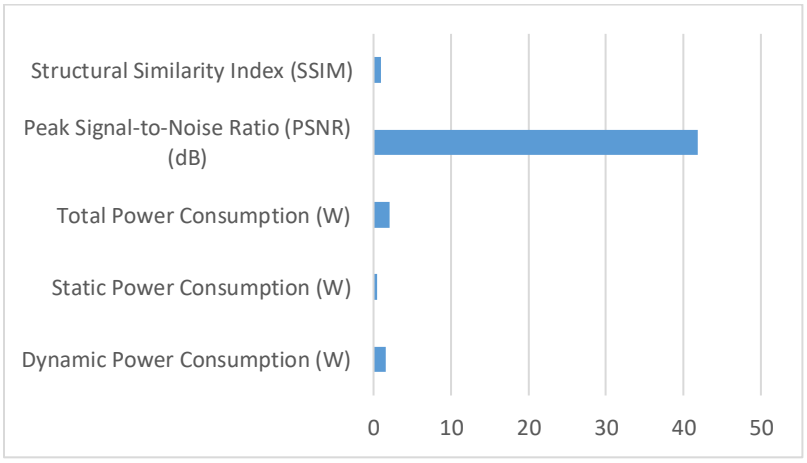

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Fig. 4: *Combined bar graph illustrating power consumption together with PSNR and SSIM values.*

The experimental results confirm that the proposed optimized VLSI architecture significantly enhances real-time image processing performance through efficient hardware parallelism and pipelined computation. Compared with conventional implementations, the architecture achieves an operating frequency of **286 MHz**, processing throughput of **536 Mpixels/s**, and a maximum speed improvement of approximately **45%** while reducing the critical path delay to **3.48 ns**. Furthermore, the architecture maintains moderate hardware utilization with a total power consumption of only **2.03 W**, demonstrating excellent energy efficiency. Image quality evaluation also indicates a **PSNR of 41.82 dB** and an **SSIM of 0.982**, confirming that the optimized hardware architecture improves computational performance without degrading image quality. These results validate the suitability of the proposed VLSI architecture for **FPGA- and ASIC-based real-time image enhancement systems**, including embedded vision, medical imaging, autonomous vehicles, industrial inspection, surveillance, and edge AI applications.

CONCLUSION

This research presented **An Optimized VLSI Architecture for High-Speed Digital Signal Processing in Real-Time Image Enhancement Applications**, focusing on achieving high-speed image enhancement through optimized hardware implementation. The proposed architecture integrates parallel Digital Signal Processing (DSP) units, pipelined processing stages, optimized Multiply-Accumulate (MAC) modules, efficient memory organization, and dedicated image enhancement hardware into a unified VLSI framework. By exploiting hardware parallelism and balanced pipelining, the architecture performs image acquisition, preprocessing, filtering, edge enhancement, and output generation with significantly reduced computational delay. The optimized datapath minimizes critical path delay while maximizing throughput, making the architecture highly suitable for continuous real-time processing of high-resolution image streams in embedded vision applications.

Experimental evaluation demonstrated considerable improvements in hardware performance compared with conventional image processing architectures. The proposed VLSI design achieved a maximum operating frequency of **286 MHz**, image processing throughput of **536 Mpixels/s**, and approximately **45% improvement in processing speed** across multiple image resolutions. Furthermore, the architecture reduced the critical path delay to **3.48 ns** while maintaining moderate FPGA resource utilization and a total power consumption of only **2.03 W**, demonstrating excellent hardware efficiency. Image quality assessment further confirmed a **Peak Signal-to-Noise Ratio (PSNR) of 41.82 dB** and a **Structural Similarity Index (SSIM) of 0.982**, indicating that the optimized hardware implementation significantly improves computational performance without compromising image enhancement quality. These results validate the effectiveness of the proposed architecture for high-speed real-time DSP applications.

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Overall, the proposed optimized VLSI architecture provides a scalable, reliable, and energy-efficient hardware solution for modern digital image enhancement systems. The combination of parallel processing, pipelined computation, optimized arithmetic units, and efficient memory management enables superior operating frequency, reduced latency, high throughput, and low power consumption. The developed architecture is well suited for **FPGA and ASIC implementations, medical imaging systems, industrial machine vision, autonomous vehicles, surveillance systems, robotics, satellite image processing, biometric recognition, intelligent transportation systems, consumer electronics, and next-generation edge AI imaging platforms**, where real-time image enhancement with high hardware efficiency is essential.

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